EEE 433/591 Fall 2012 Lab 5 LDO Regulator Design

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Lab objective:

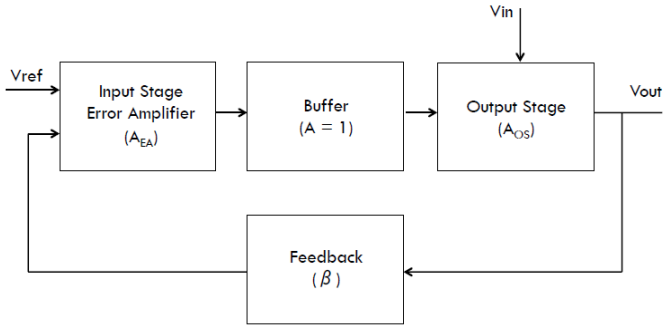
The Low Dropout Regulator (LDO) is a kind of linear voltage regulator which controls the voltage and current using transistor as variable impedance elements. It is commonly used in portable equipment due to the low noise and fast transient response. In this lab, we are going to design, simulations, and analysis of low-dropout regulator.

Requirements:

- Voltage supply 2.5 V, 0.35 Micron CMOS Process
- Delivers 20 mA current
- Amp Gain: 30 dB, Pick V_{DSAT} – 0.25 V
- Output Regulated Voltage of 1.5 V
- tsmc25N NMOS (k'n=274.75uA/V^2 and Vtn =0.49 V)
- tsmc25P PMOS (k'p=95.75uA/V^2 and Vtp=0.54V)

Analysis:

The LDO basic structure contains four parts: input stage (or error amplifier), buffer, output stage.



The output voltage based on the figure 1 can be derived as the equation :

$$V_{OUT} = \frac{V_{REF}\left(A_{EA}A_{OS}\right)}{1+\beta\left(A_{EA}A_{OS}\right)} + \frac{V_{IN}}{1+\beta\left(A_{EA}A_{OS}\right)} \approx \frac{V_{REF}}{\beta} + \frac{V_{IN}}{\beta\left(A_{EA}A_{OS}\right)}$$

It shows that the load regulation is limited by the open loop current gain of the system, as noted from above equation, if the A_{EA} is much larger, the LDO have a greater ability to maintain the specified output voltage under varying load condition, that is, $V_{OUT} = V_{REF}$.

In the LDO schematic diagram, either NMOS or PMOS can be used as pass device. In this lab, NMOS transistor is chosen because of its low output impedance and easier compensate.

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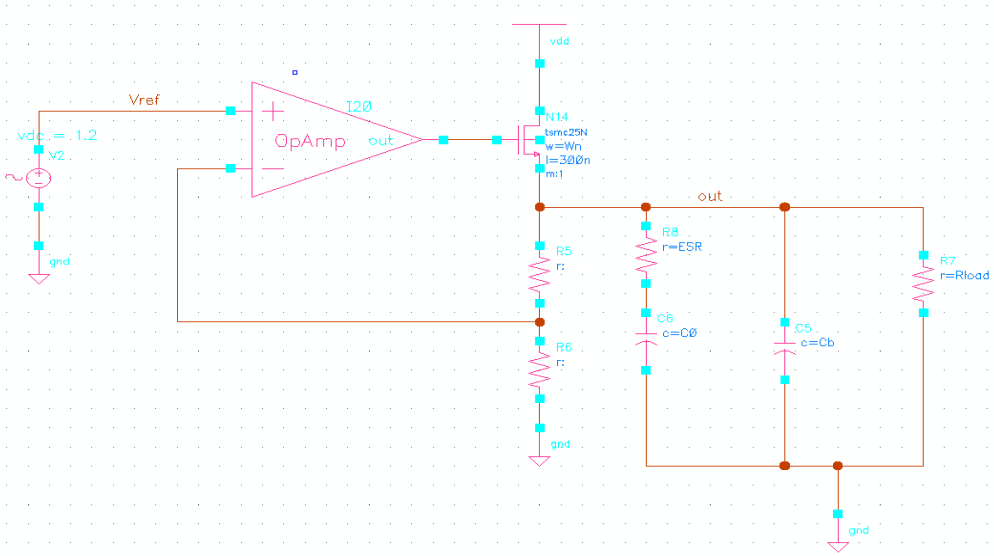

The LDO Poles and Zeros are the function of output capacitor (C_0), the equivalent series resistance (ESR) of the output capacitor, and the bypass capacitor (C_b). To decrease the voltage variation resulting from the load transient, a big value of output capacitor and the low ESR of the capacitor are selected as following table:

output capacitor (C_0)	1uF
equivalent series resistance (ESR)	0.5Ω
bypass capacitor (C_b).	0.1uF

- **Determine device sizes, currents, and DC/AC values**

  (1) Error amp

  As mentioned above, the gain of amplifier should be as large as possible in order to maintain the stability of LDO regulator. The amplifier design is similar to the previous lab. The active load MOS amplifier is applied. The lab III differential amplifier composes with current mirror circuit and the differential pair circuit. The mirror **biasing current supply is 10mA**. And **the DC voltage is 1.2 V** as reference voltage. AC **signal** for transient simulation is set as **10mA**. The parameters of COMSFET are listed as below table in order to meet the requirement of **$I/2 = I_1 = I_2 = 5uA$.** V_{DSAT} is set to be **$V_{DSAT} = 0.25$ V,** therefore**, $V_{GS1,2} = 0.15+0.5 = 0.65$V.** As requirement, **$I = 10$ uA,** so **$I/2 = I_1 = I_2 = 5uA$.** Though the $I_{DS} = 1/2*k'n*(Wn/Ln)*(V_{DSAT})^2$, we get our initial W for nmos and pmos values:

Wn	**1.39um**	Ln	**1um**
Wp	**485nm**	Lp	**1um**
Wn_buffer	**450nm**	Ln_buffer	**1um**
Wp_buffer	**450nm**	Lp_buffer	**1um**

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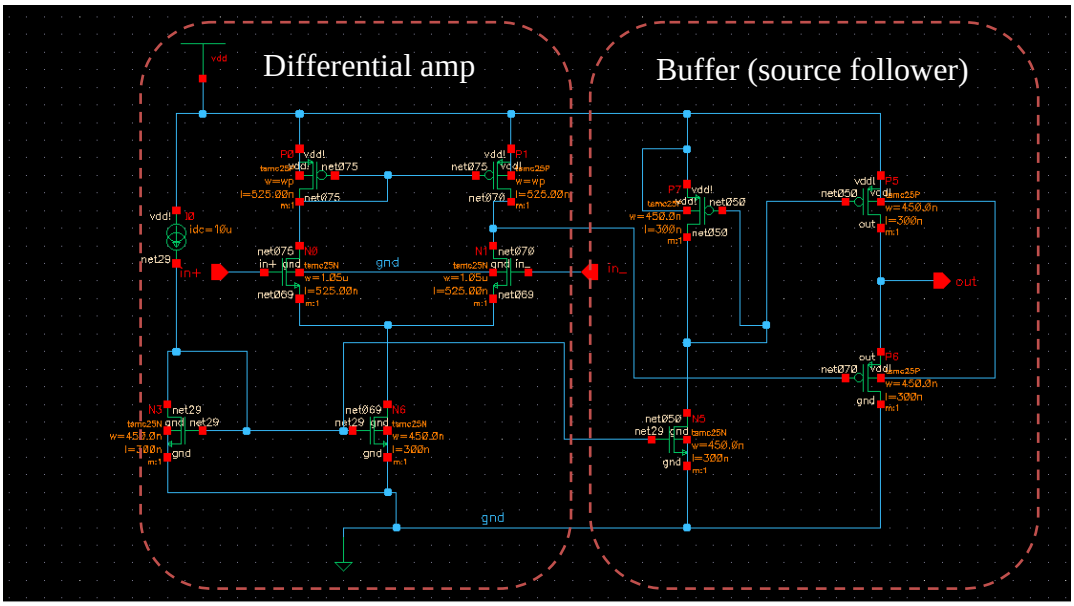
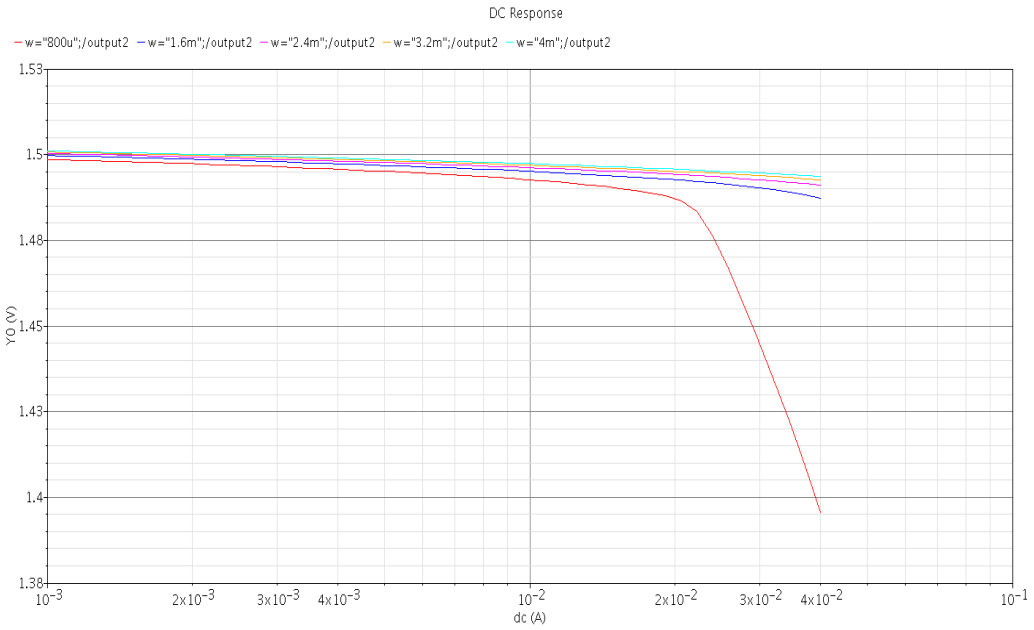


(2) Pass transistor

The size of pass transistor is done by calculating the saturation equation with current = 20 mA, V_S = 1.5 V and V_D = 2.5 V. V_{DSAT} = 0.25 V.

From the saturation equation: **$I = 0.5*k'n(Wn/Ln)*(V_{SAT})^2$**, the **Wn = 1.2mm.** The **V_{out} vs I_{load}** simulation, as shown below, also indicated the range of the Wn. The output voltage is relative stable when the Wn is above 800um. The plot indicates the larger Wn have more stable output voltage.



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- **Perform DC operating point and AC analysis**

The DC parameters of each transistor for amp are summarized as below:

	V_{DSAT} (V)	I (uA)	V_{GS} (V)	Region
N0	**0.25**	**5**	**0.65**	**Sat**
N1	**0.25**	**5**	**0.65**	**Sat**
P0	**0.25**	**5**	**0.15**	**Sat**
P1	**0.25**	**5**	**0.45**	**Sat**
P point	**0.25**	**10**	**0.787**	**Sat**

The AC parameter is calculated by simulation of the NMOS and PMOS using calculated W/L, the output impedance is the inverse slope of V_{DS}- I_{DS} curve, as shown in the figure below.

	NMOS	PMOS
Slope of V-I curve	**$1.4*10^{-6}$**	**$1.19*10^{-7}$**
r_o	**$7.1*10^5$**	**$84*10^5$**
rin	**infinite**	**infinite**

In Saturation region, $\mathbf{g_m = \frac{\partial I_D}{\partial V_{GS}} = k'n(Wn/Ln)*(V_{SAT}) = 2I_{DS}/V_{DAT} = 6.66*10^{-5}\ S.}$

From this we can get the $\mathbf{A_V = g_{m1,2}*(r02//r04) = 6.66*10^{-5}*(7.1*10^5//84*10^5)=43,\ (A_V)_{dB} = 32dB}$

- **Find approximate values the caps Cgs, Cgd of the pass transistor**

The values of Caps from "results browser" of Cadence, or use approximate value C=WL*Cox, the result is

Cgs	**2.346pF**
Cgd	**0.852pF**

- **Estimate the poles, specially the output pole W_{PL}**

The resulting output poles calculation is provide in the section 8 of **Technical Review of LDO Operation and Performance** by Texas Instrument. As a summary, the approximated poles and zero are given by

$$P_o \approx \frac{1}{2\pi R_{ds} C_o} \approx \frac{I_L}{2\pi V_A C_o}$$

$$P_b \approx \frac{1}{2\pi R_{ESR} C_b}$$

$$P_a \approx \frac{1}{2\pi R_{par} C_{par}}$$

Where R_{ds} is the r_0 for the pass transistor $1/g_{ds} = 1/(5.05*10^{-3})=200\Omega$, *Rpar* and *Cpar* are the output impendence of amplifier.

$\boldsymbol{P_0}$	**795 Hz**
$\boldsymbol{P_b}$	**3.1GHz**
$\boldsymbol{P_a}$	**97.05KHz**

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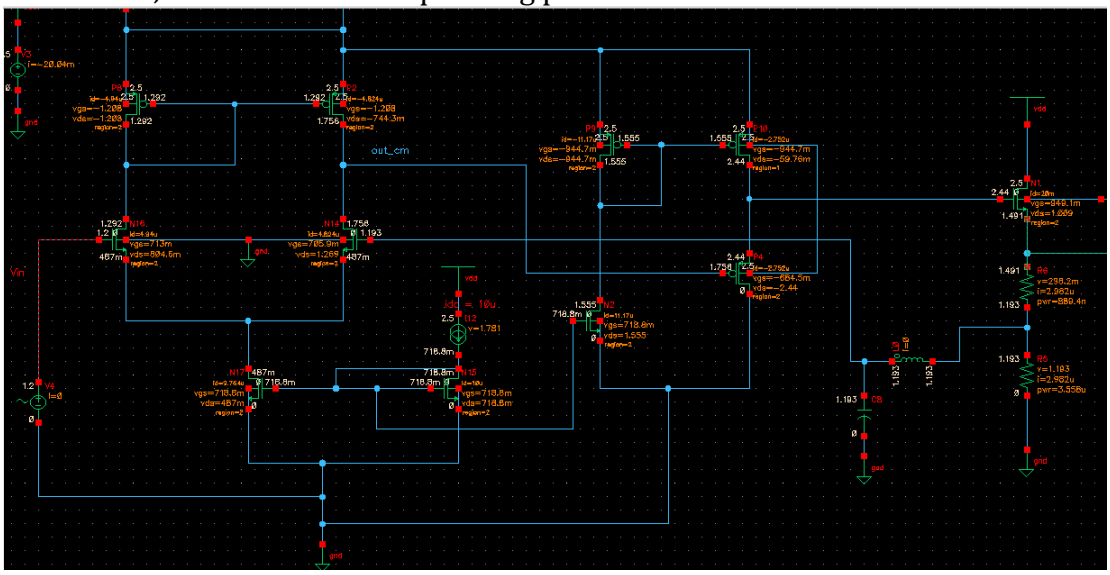
Simulations:

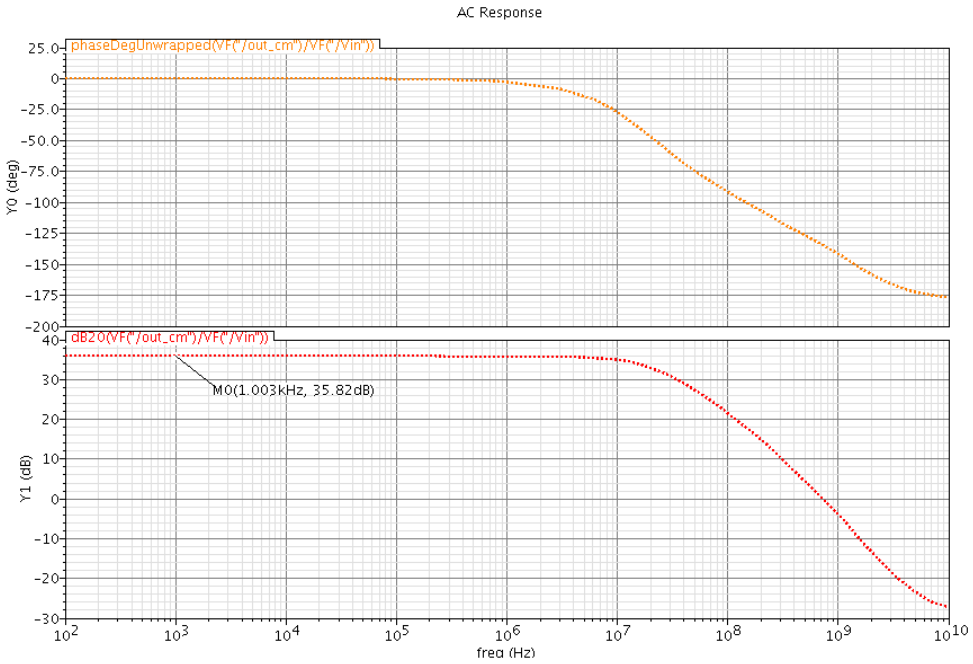
- **DC Operating point analysis**

  By adding the inductance L=1G H and the capacitance C=1M F to break the feedback loop. At the AC input 10mA at 1KHz. the Error amp open loop gain is obtained, as well as the DC operating point of LDO.



The region analysis shows the size settings of the NMOS and PMOS are appropriate, because the transistors are working at saturation region.

The open loop gain reach to 35 dB, as shown below:



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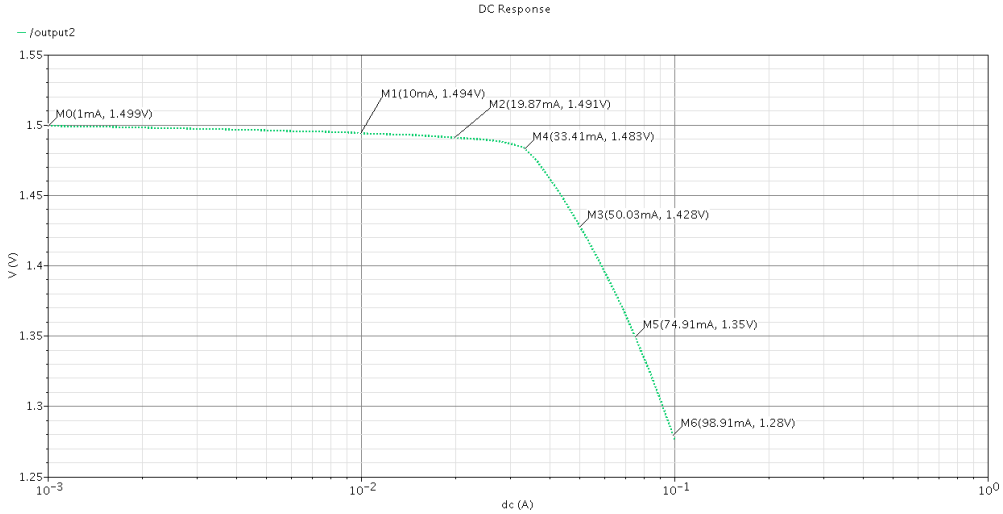
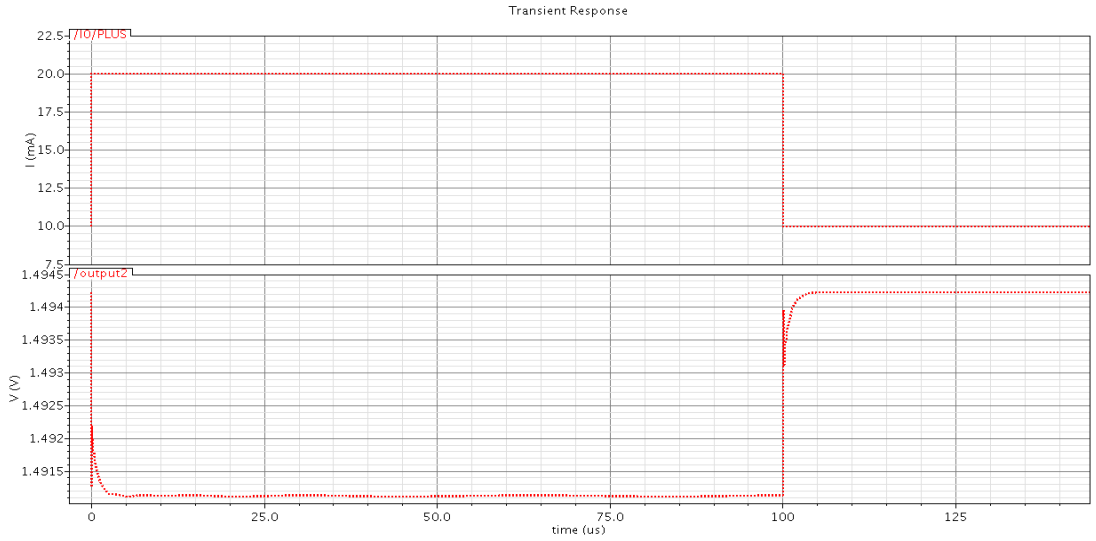
- **Plot V_{out} vs I_{load}. I_{load} can be given as a DC current source. Sweep I_{load} parametrically from 1mA to 100mA and plot V_{out} at pass transistor W is 1.2um. Find the % change in V_{out} over the entire range of load currents**

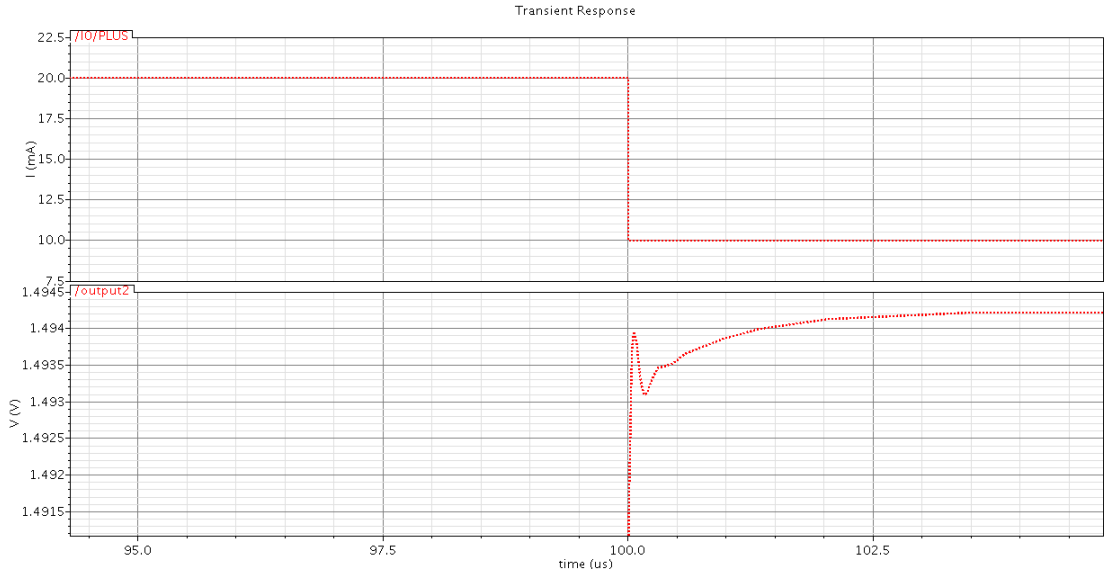


From the V_{out} vs I_{load}**,** the % change in Vout from **1mA to 33mA** is (1.483-1.499)/1.499 =**1%**. However, once the current goes above 33mA, it drops dramatically, (1.28-1.499)/1.499=**14.6%**

- **Transient response .Give a step change of 10mA to 20mA at the load and observe the transient output voltage for 1ps rise time**

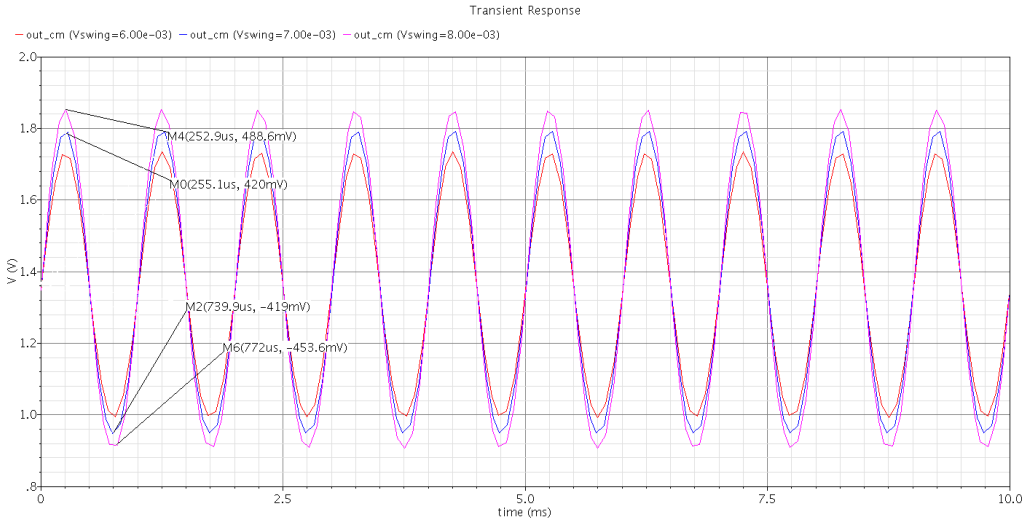


Zoom in the output plot:



The plot shows that it takes time for the LDO to response to a load current step. The current initially comes for capacitor, hence the output drops. Once the LDO current equals the load current the output voltage stops decreasing. The LDO current then charges the capacitance. This overshoot happens because the compensation design.

- **Show the maximum output signal swing(in transient simulations) at the output of the amplifier**



The maximum without distortion will be **420+420=840 mV**

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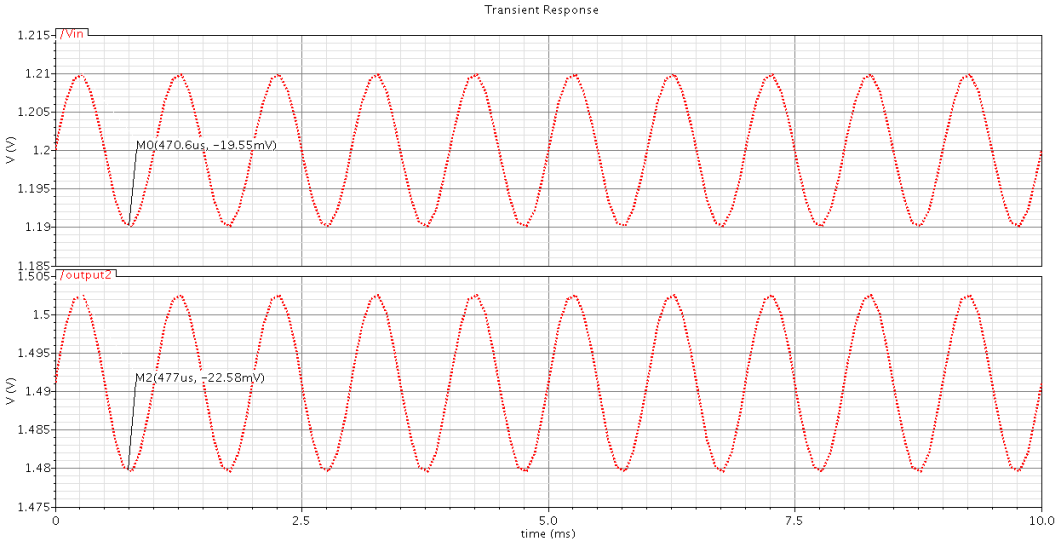
- **Input a 1KHZ Tone and plot the output in time.**



The output follows the input current with no phase change. The amplitudes of input and output are almost at the same values, which proves the feedback loop effectively regulate the output voltage.

Comparison: **Compare Analysis with Simulations. Discuss the Quiescent current (the current flowing through the resistor divider, in no load condition), & the efficiency of the circuit.**

The analysis agrees with simulation result. It shows the gain as 35dB very close to analysis value 32 dB. The analysis saturation size of transistors also been verified in simulation.

For the MOS transistors, there is almost zero current flowing through the resistor divider due to the very large resistor. The Quiescent current has a near constant value with respect to the load current. The only things that contribute to the quiescent current for MOS transistor are the sampling resistor and error amplifier. Considering about the power consumption, LDO with MOS transistors are essential to achieve lower power consumption. The power dissipation of LDO accounts for the efficiency, because Efficiency = $(I_O*V_O)/((I_O+I_Q)*V_I)$ and power disspation =$(V_I-V_O)/I_O$. If the circuit has a high quiescent current, the efficiency will be low. Therefore the minimum quiescent current is necessary for maximum current efficiency.